Design of CAM Controller for Improved Match Ratio with Built-in Comparison Fault Testing

Hima Sara Jacob, Nandakumar.R, Arathy.S

Abstract— Content Addressable Memory (CAM) is a special purpose Random Access Memory device that can be accessed by searching for data content. In this paper Xilinx® CAM v 6.1 is the target memory. The CAM controller is used to control the CAM memory through interface. Replacement policies are used to improve the hit ratio. Testing of the memory is essential to ensure quality and to increase reliability. This paper describes a novel architecture design of CAM Controller with sequential replacement policy, so as to improve the match ratio of the CAM memory. A fault testing module is also included in this design for testing the comparison fault occurring in the CAM memory.

Index Terms—Associative memory, Content Addressable Memory, Fault, Hit ratio, Match ratio, Sequential replacement policy, Testing.

1 INTRODUCTION

Content Addressable Memory (CAM) is an outgrowth of Random Access Memory (RAM) technology and in order to understand CAM, it helps to contrast it with RAM. A type of memory commonly used in many types of switching circuits is a Content Addressable Memory (CAM).Compared to a Random Access memory (RAM), a Content Addressable Memory (CAM) has a unique method of accessing data words within the memory. In a Random Access memory, during a read operation an address is supplied that uniquely identifies one location within the memory. The memory responds with a data word stored in the addressed memory location. The Content Addressable memory is a special purpose Random Access Memory device that can be accessed by searching for data content. For this purpose, it is addressed by associating the input data, simultaneously with all the stored words and produces output signals to indicate the match condition between the input data and the stored words. This operation is referred to as association or interrogation and this type of memory is also known as Associative memory [2].

In this paper a novel architecture design of a CAM Controller with replacement policy and a buit-in testing module for testing the comparison fault of CAM memory is described. Replacement policies are used to improve the "hit ratio" of the memory [3],[4],[5].In order to improve reliability testing of the memory is needed [6],[7],[8],[9].[10]. In this paper sequential replacement policy [3] is used to improve the "match ratio" of the CAM memory. The CAM memory targeted in this design is Content-Addressable Memory v6.1 by Xlinx® [1].The CAM core is a fully verified memory unit that uses content matching rather than addresses. The core enables faster data searches as compared to other memory implementations and offers parallel content compares to find a valid address. The width, depth, memory type and other optional features of the CAM core can be customized to fit wide variety of applications. The CAM used here is 256x16 and memory type is Block RAM. Since the memory type is Block RAM the write operation takes two clock cycles latency and read operation has one clock cycle latency [1].The match address type is binary encoded and lowest match address resolution is selected. Memory initialization is done as described in [1].

The paper is organized as follows: The proposed Controller architecture is referred in section 2; Conclusion is given in section 3.

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2 PROPOSED CONTROLLER ARCHITECTURE

2.1 Introduction

The CAM controller is designed to work with CAM version 6.1 of Xilinx®.It has a user interface on one side and the memory on the other side. The controller architecture consists of Control unit, Data path & Address unit, a built in Replacement block, so as to improve the match ratio of the memory and a Testing unit for the purpose of testing the memory.

2.2 Block Diagram

The CAM controller is used to control the CAM memory through interface. The block diagram for the controller along with the CAM memory is shown in Figure 1.The controller consists of Control unit, Data path & Address unit, Replacement block and a Testing module.

The CONTROL SIGNALS from the control unit are given to the memory and also to the Data path & Address unit. The DATA INPUT and the SEARCH INPUT to the controller is 16 bit. The ADDRESS is 8 bit. The CONTROL INPUT is the user command to the controller and it is of 2 bit. The sys_clk and reset signal is also given to the controller. The DATA BUS and CMP_DATA_BUS from the controller to the memory is 16 bit. The ADDRESS BUS is 8 bit. The control signals to the memory and the Data path & Address unit are "en" (enable) and "we" (write enable) signals.

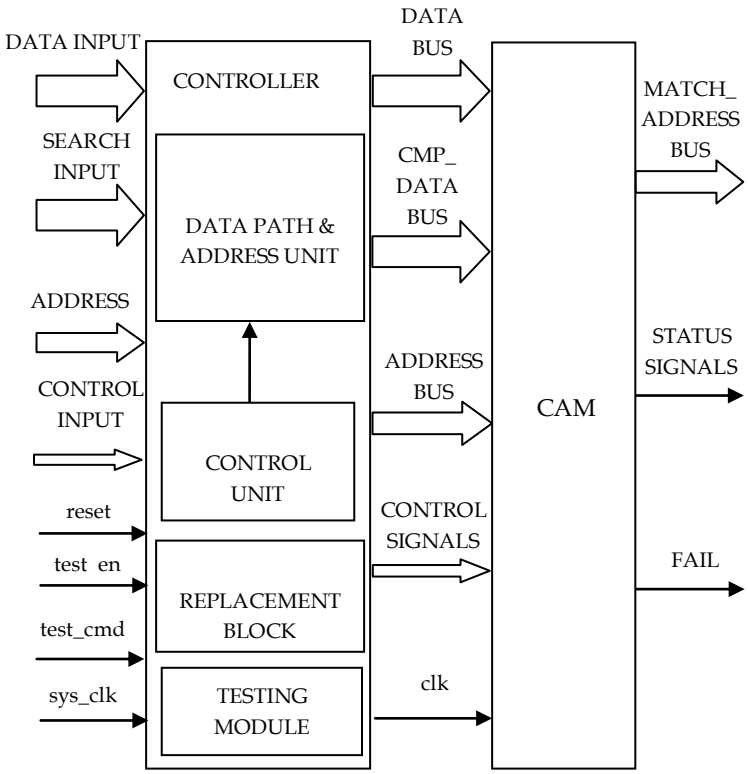

Figure 1: Block Diagram

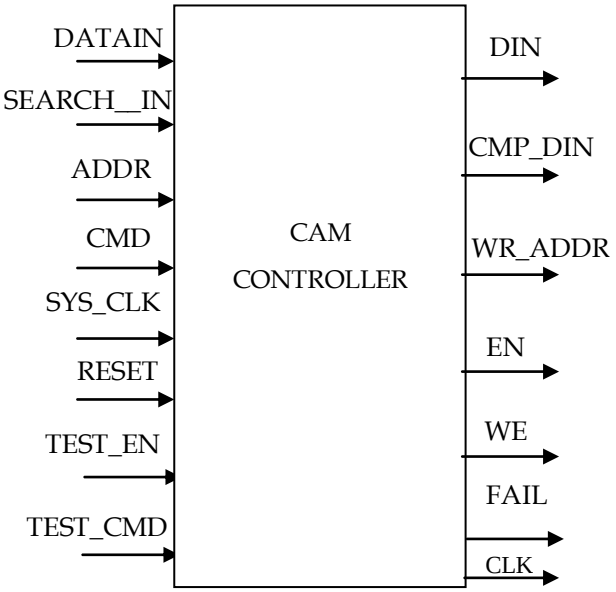

Figure 2: Input/output diagram for the Controller

The MATCH_ADDRESS BUS indicates the address that matches the contents of the CMP_DATA_BUS.Status signals are "busy", "match", "single_match" and "multiple_match".The "busy" signal will be asserted during a write operation and will be low during read operation. The "match" signal will be asserted when the data on the CMP_DATA_BUS matches data in one or more locations in the CAM. When more than one match is present in the CAM "multiple_match" signal is asserted and when there is only one match "single_match" signal is asserted. During read operation when the data is not present in any of the memory locations, then the "match" signal will be low. At that time the replacement block will carry out the replacement of the data in a sequential manner starting from the first location.

Testing module is used for testing comparison fault in the CAM memory. During testing the normal operation of the controller will be suspended and the controller will be in the testing mode.

2.3 Pin Description

The Input/output diagram for the controller is shown in Figure 2.The output ports from the controller are given as input ports to the memory.

All the pins in the Input/output diagram of the controller are described in Table 1. The direction and the description of the pins are also given.

The pin description for the controller is given below

TABLE 1: Pin description

Port Name	Direction	Description
SYS_CLK	Input	All the operations are synchronous to the rising-edge of the system clock input
RESET	Input	This is used to reset the controller and the memory
DATAIN	Input	This is the 16 bit data given to the controller during write operation
SEARCH_IN	Input	This is the 16 bit data given to the controller during read operation
CMD	Input	This is the 2 bit command signal given to perform various operations.
TEST_EN	Input	This is the 1 bit test enable signal to enable testing
TEST_CMD	Input	This is the test command signal to per-

		form read and write operation for testing.
ADDR	Input	This is the 8 bit address given to the controller during write operation
DIN	Output	Data to be written to the CAM ,by the controller during write operation
CMP_DIN	Output	Data to look up from the CAM during read operation
WR_ADDR	Output	The location that the data on DATA BUS will be written into the CAM
EN	Output	Control signal used to enable both write and read operation
WE	Output	Control signal used to enable transfer of data into CAM from the DATA BUS. During write operation "WE" is high and during read operation it is low
FAIL	Output	This signal is used to inform the user whether there is a fault or not
CLK	Output	All the operations are synchronous to the rising-edge of the clock input to the memory.

2.4 Detailed Architecture

The complete architecture of the controller along with the memory is shown in Figure 3.

In this era of fast processors and processors with many cores, there is a requirement for faster and bigger memories. But today the speed of memories is not able to match up with the speed of processors. So there is the need for fast memory controllers. Memory controller is used to control the memory through interface. The controller is expected to synchronize the data transfer between the processor on one side of the controller and the memory on the other side.

CAM Controller designed in this paper consists of Control unit, Data path & Address unit, Replacement block, Select logic, Testing Module and Test / Normal mode select logic. Each and every unit given in Figure 3 is explained below.

A. Control Unit

This unit is responsible for generating the control signals to the memory and the Address & Data path unit.The control signals generated by the control unit are "en" (enable) and "we" (write enable).The command input "cmd" is given to the control unit by the processor. The controller has a transition through four states .When the given command input is "cmd=00" controller will be in the IDLE state. At this time en=0 and we=0.The write and read operation can be performed only if the "en" signal is high. The command input for write operation is "cmd=01". At this time en=1 and we=1 and controller is in the WRITE state. The command input for read operation is "cmd=10" .At this time en=1 and we=0 and the controller is in the READ state.

B. Data path & Address Unit

This unit of the controller consists of Data register, Comparand register and Address register. The Data register is for the storage of input data to the controller, during write operation. At the rising edge of the system clock the data at the DATA INPUT BUS will be available at the DATA BUS. At this time the control signals en=1 and we=1. This register is of 16 bit and a parallel in parallel out (PIPO) register can be used. The Comparand register is meant for the storage of data during a read operation. At the positive edge of the system clock the data at the SEARCH INPUT BUS will be available at the CMP_DATA BUS. At this time en=1 and we=0.Comparand register used here is a 16 bit PIPO.The Address register is used during write operation and it is an 8 bit PIPO register. The input address will be available at the ADDRESS BUS during the rising edge of the system clock and at this time en=1 and we=1.The "match_addr" is the CAM address where matching data resides. The "match"signal indicates that at least one location in the CAM contains the same data as the DATA BUS. The "single_match" signal indicates the existence of matching data in one location of the CAM. The "multiple_match" signal indicates the existence of matching data in more than one locations of the CAM. The "busy" signal indicates that a write operation is currently being executed.

C. Replacement Block

This unit is responsible for the replacement of the data in the memory location so as to improve the match ratio of the memory. A sequential replacement policy is used here. This Replacement policy is simple to implement and consumes only little power [3]. When the controller is in the read state the data at the SEARCH INPUT BUS will be available at the CMP_DATA BUS .The memory locations will be searched simultaneously for the data. If the data is not present in any of the memory locations then the "match" signal will be low. Then the replacement block will be active. The replacement block simply increments an address counter sequentially to points to the location of the new entry [3].Then the search input data will be written to that location. To perform this

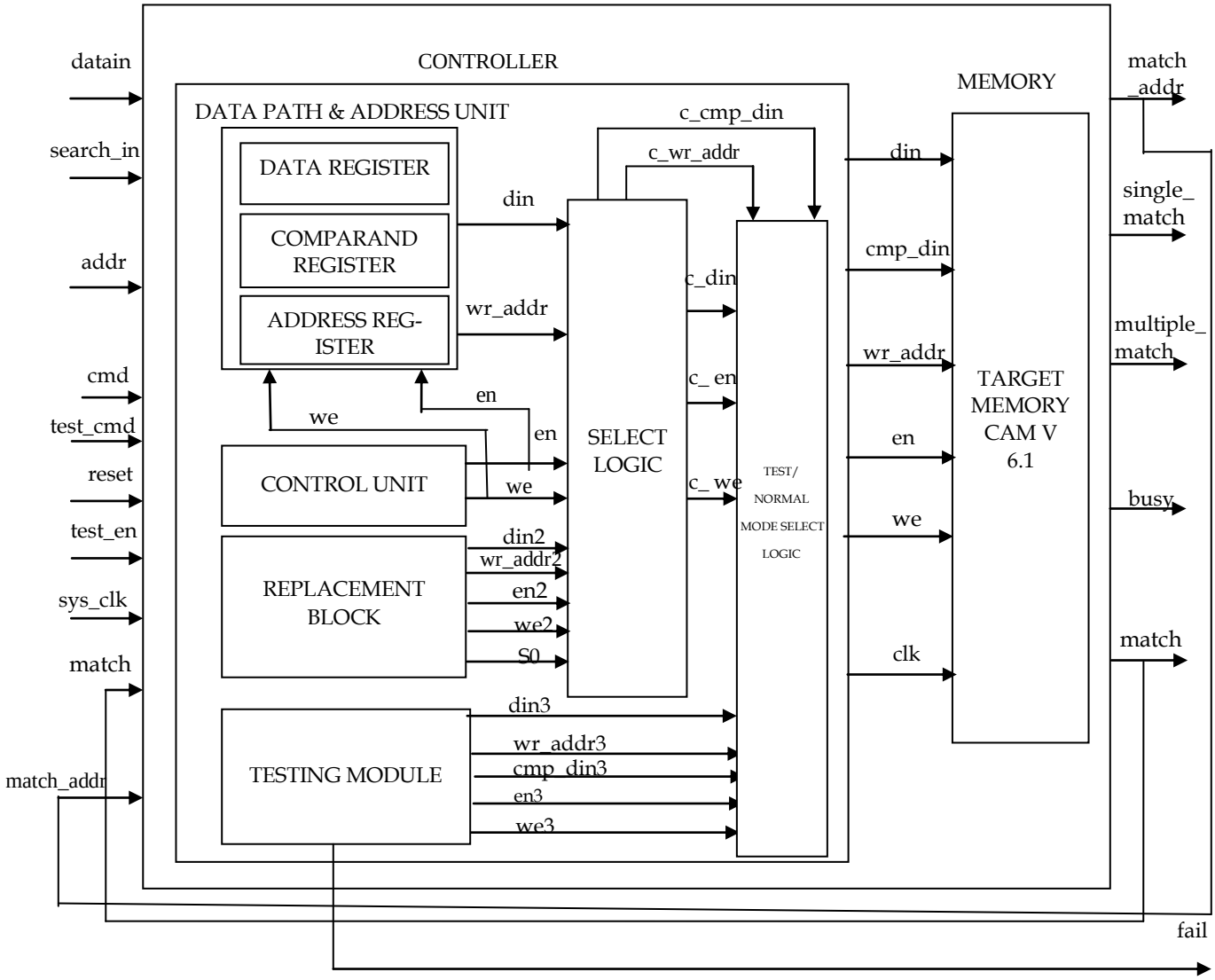

Figure 3: Controller Test Environment Architecture

replacement the "en" and the "we" signal should be high and after replacement "we" signal becomes low.

D. Select Logic

This unit is responsible for selecting either the outputs from the replacement block or the outputs from the control unit and data path & address unit. The output from the replacement block is selected if the data that is searched for is not present in any of the memory locations. At this time the "S0" signal will be high. The outputs from the control unit and data path & address unit will be selected when the data that is searched for is present in any of the memory locations and at this time "S0" signal will be low.

E. Testing Module

This module is meant for testing the CAM memory. During testing the test_en (test enable) signal will be high and the controller will be in the test mode. Test commands (test_cmd) are used for performing a sequence of read and write operations. The most important fault that can be occur in the CAM memory is Comparison fault [6].In case of testing, first a write operation and then a read operation has to be performed to every memory locations and each memory location is written and read several times. The "fail" output in the architecture denotes, if there is any comparison fault or not. In-order to find whether there is a comparison fault or not, the "match" and the "match_address" is given as a feedback to the testing module and these signals are compared with the correct response. If there is any difference, then it denotes that there is Comparison fault.

F. Test/Normal mode Select Logic

This module is responsible for selecting the necessary

outputs from the testing module or from the above units during normal mode or testing mode of the controller according to the test_en (test enable) signal given. When the test_en signal is high testing of the CAM memory can be done. The test_en signal can be made low for the normal operation of the memory and can perform replacement action in case of absence of data item(s) in the memory. The required outputs from this unit are given as inputs to the memory.

3 CONCLUSION

Content Addressable Memory (CAM) is a special purpose Random Accesss Memory (RAM) device that can be accessed by searching for data content.The architecture of a custom controller for improved match ratio with built-in comparison fault testing for the Content Addressable Memory version 6.1 of Xilinx® was designed.This work is believed to serve as a good bench mark for selecting an optimum controller for the CAM memory to improve the match ratio ,to ensure quality and to increase reliability.

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